EE 505

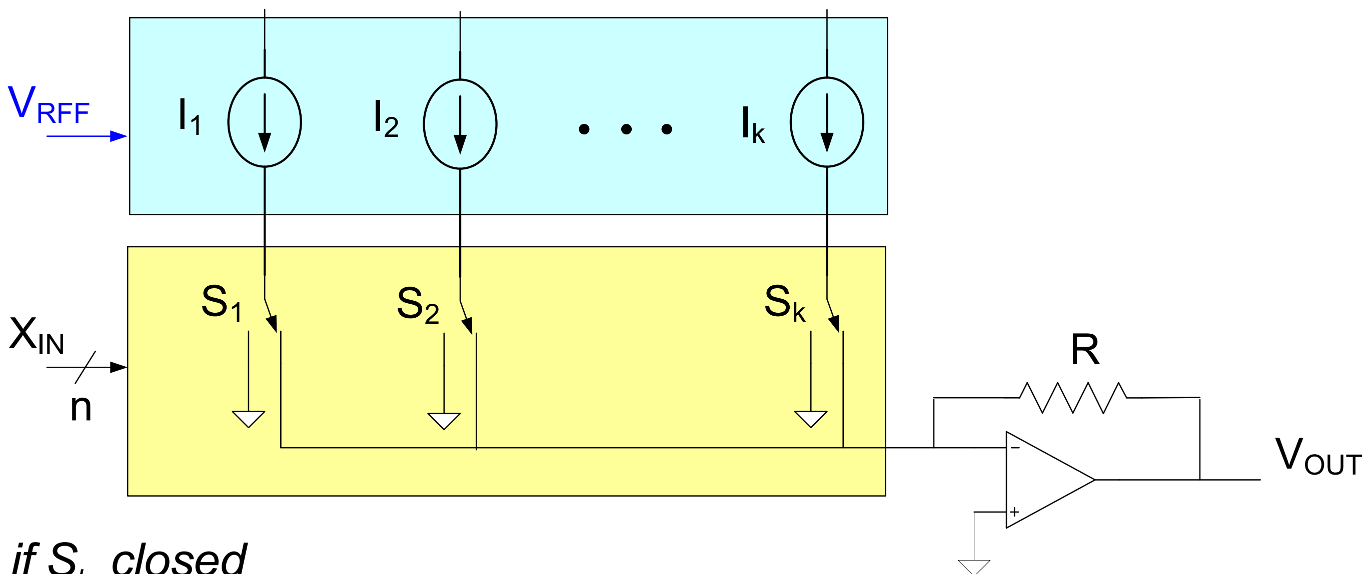
Lecture 16

Current Steering DACs

Review from Last Lecture

Current Steering DACs

Concept

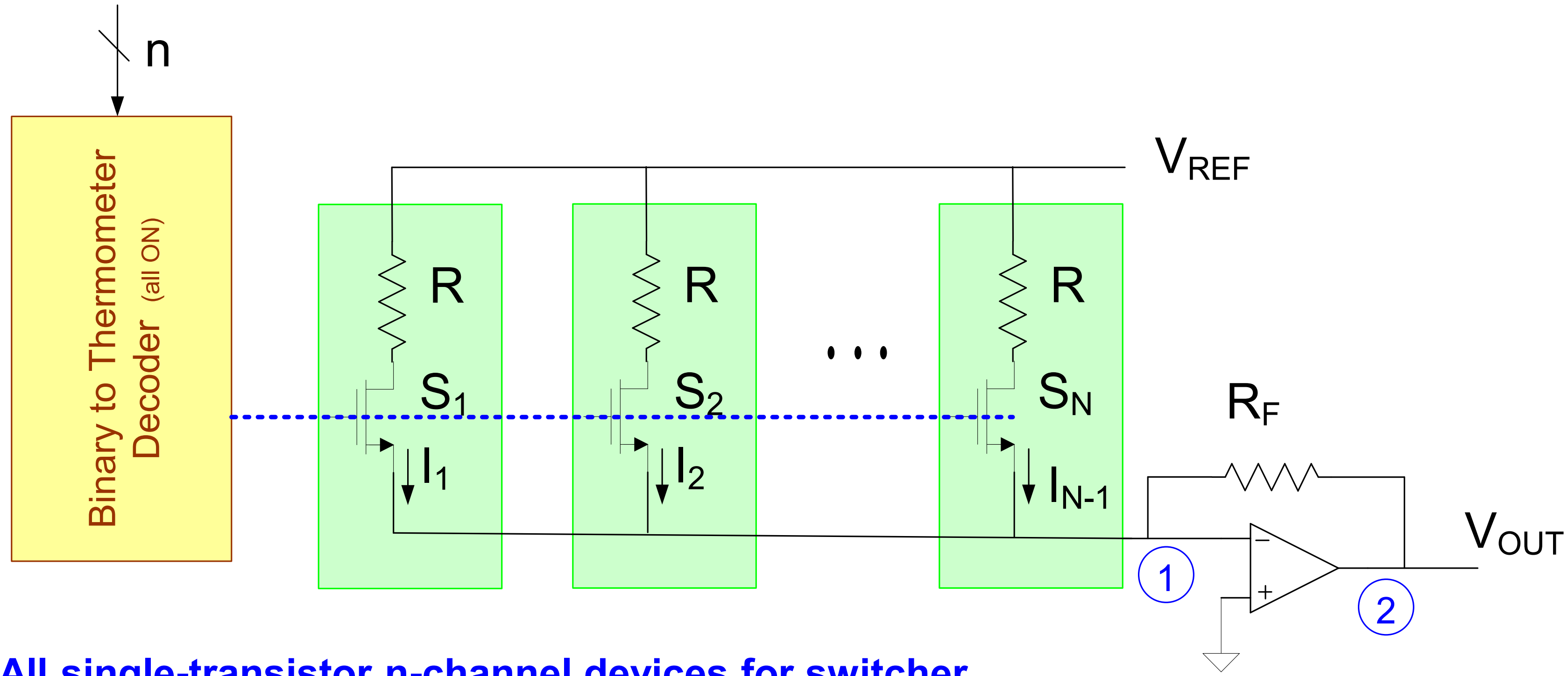


$$d_k = \begin{cases} 1 & \textit{if } S_k \textit{ closed} \\ 0 & \textit{if } S_k \textit{ open} \end{cases}$$

$$V_{OUT} = \left[\sum_{l=1}^{k} \mathrm{d_i I_i}\right](-\mathrm{R})$$

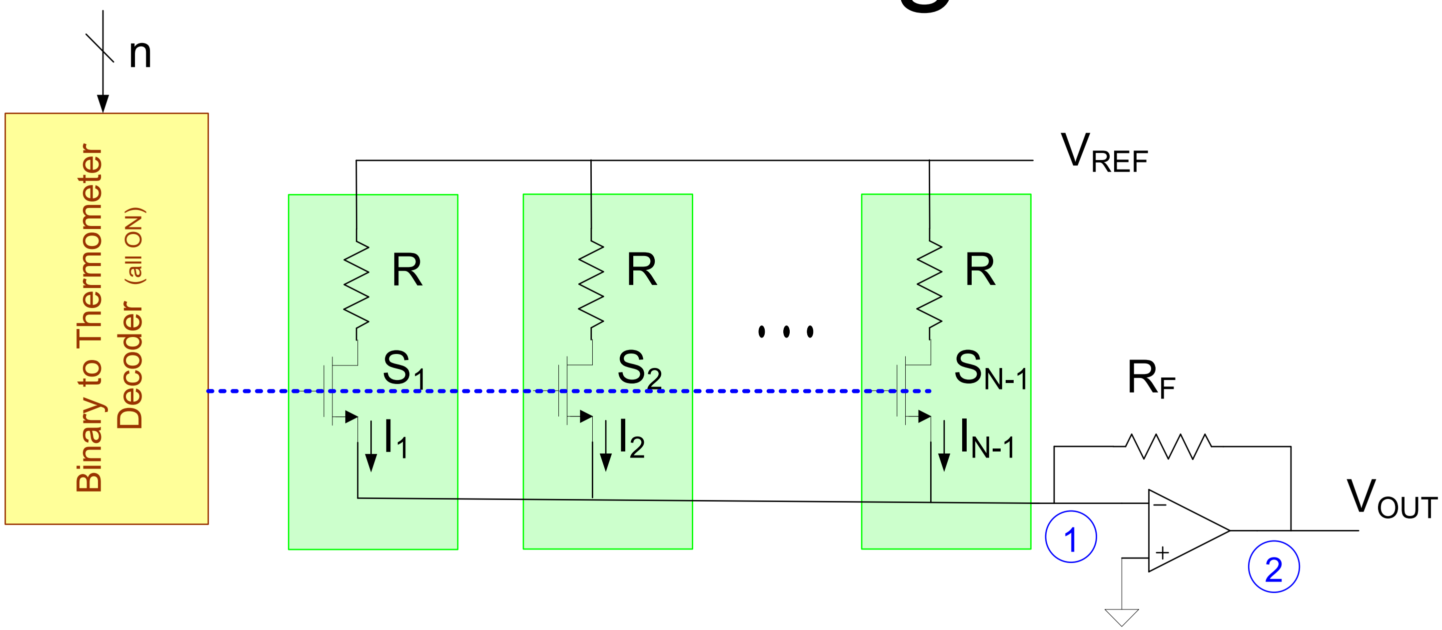
- Current sources usually unary or binary-bundled unary
- Termed bottom-plate switching
- Can eliminate resistors from DAC core
- Op Amp and resistor R can be external
- Can use all same type of switches
- Switch impedance not critical nor is switch matching
- Popular MDAC approach

Current Steering DACs



- **All single-transistor n-channel devices for switcher**
- **Unary R:switch cells**
- **Parasitic capacitances on drain nodes of switches cause transient settling delays**
- **R+Rsw is nonlinear (so nonlinear relationship between I_k and V_{REF}) but does not affect linearity of DAC**
- **Resistor and switch impedance matching important**
- **Previous code dependent transient** (parasitic capacitances on drains of switches)

Current Steering DACs



Transistor Implementation of Switches

$$\beta = \frac{\frac{R_{CELL}}{k}}{\frac{R_{CELL}}{k}+R_F} = \frac{R_{CELL}}{R_{CELL}+kR_F}$$

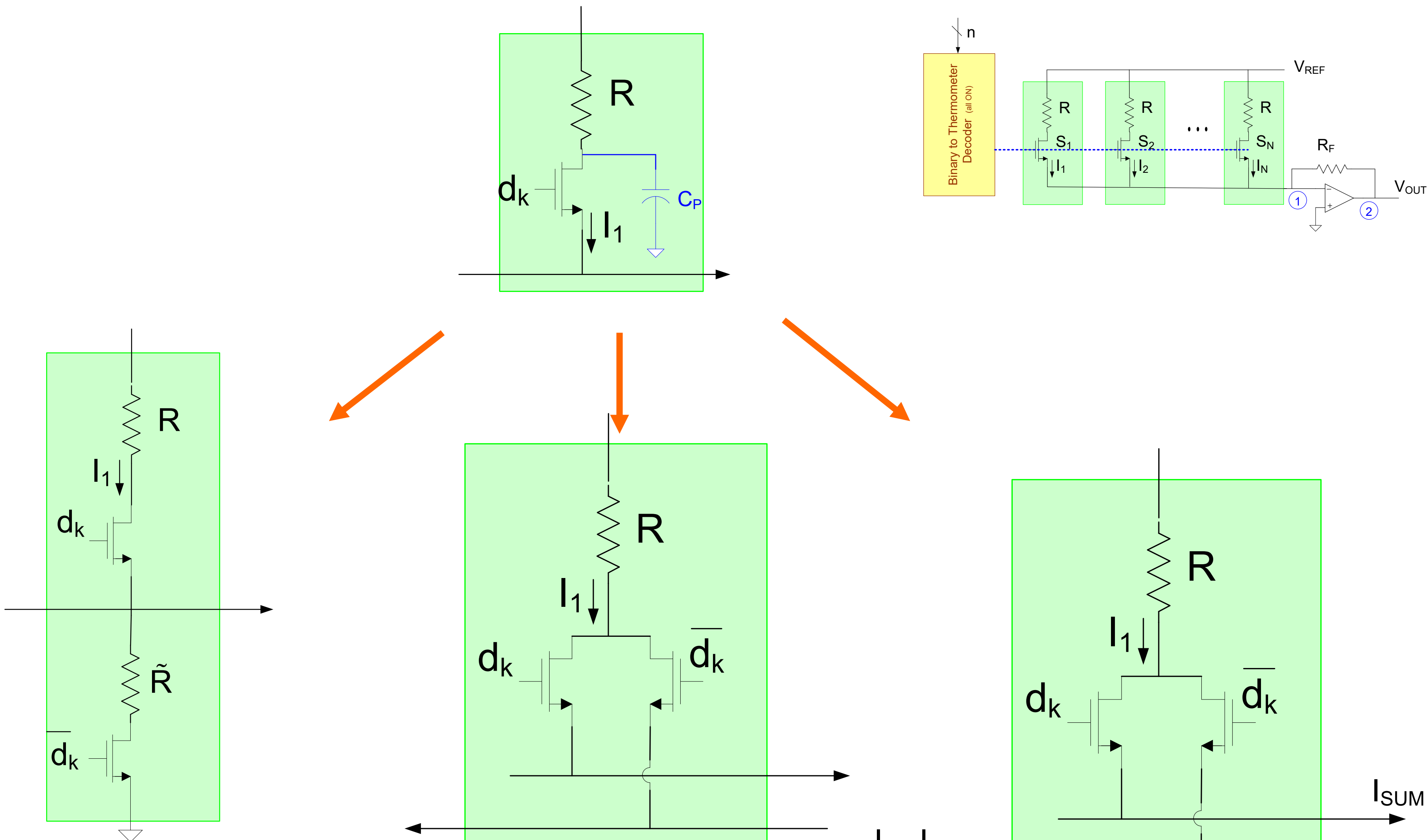
If $V_{OUTFS} = -V_{REF}\frac{N-1}{N}$ $\quad R_{CELL} = \frac{(N-1)^2}{N}R_F$

$$\frac{N-1}{2N-1} < \beta \leq 1 \quad \xrightarrow{\text{approximately}} \quad 0.5 < \beta \leq 1$$

Phase-margin code dependent so distortion will be introduced if not fully settled

Current drawn from V_{REF} changes with code (settling issues if R_{0_VREF} is not 0)

Current Steering DACs



β Compensation

(Actually static β comp)
(keeps β at approximately ½ for all codes, reduces size of compensation capacitor))

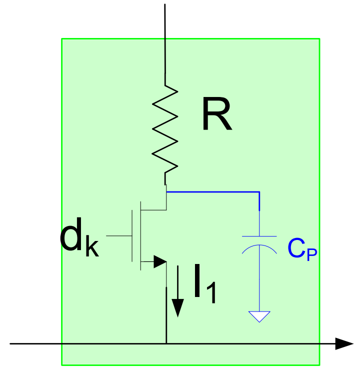
C_P Compensation

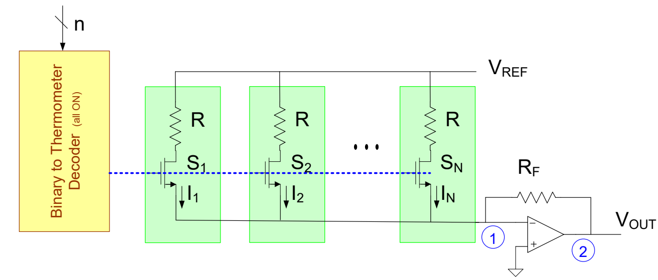
(to keep Cp from charging to V_{REF} when off)

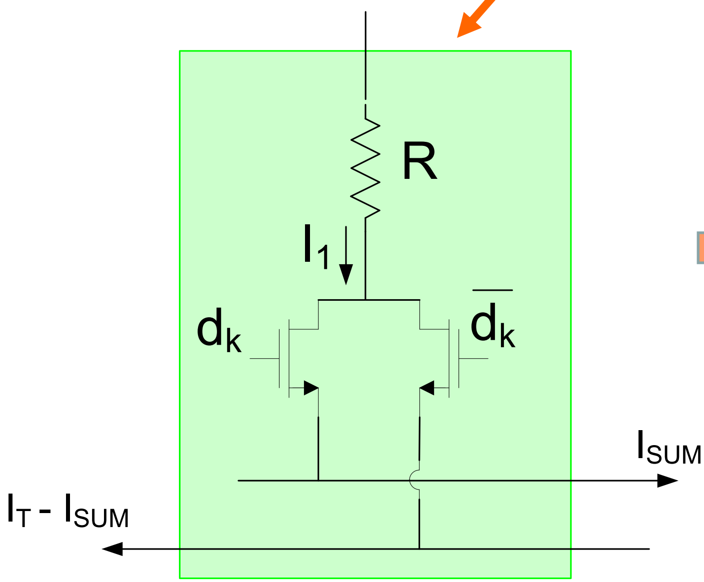
Differential Output

(inherent Cp compensation)

Current Steering DACs



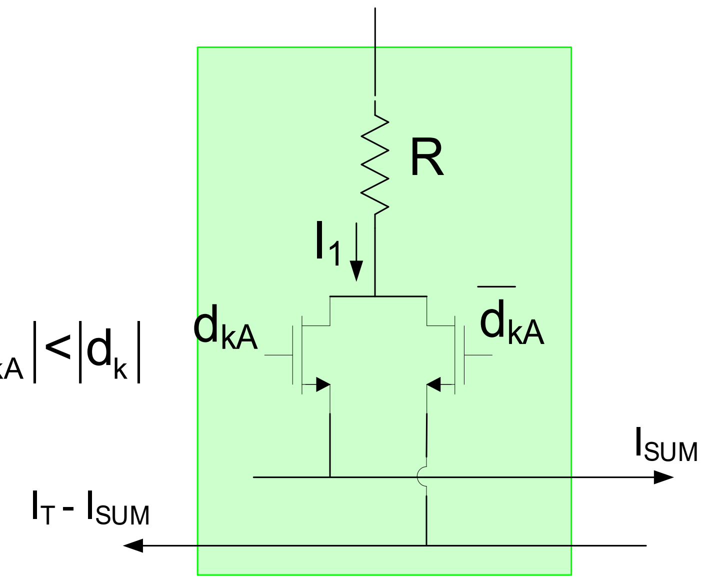




Differential Output

(inherent Cp compensation)

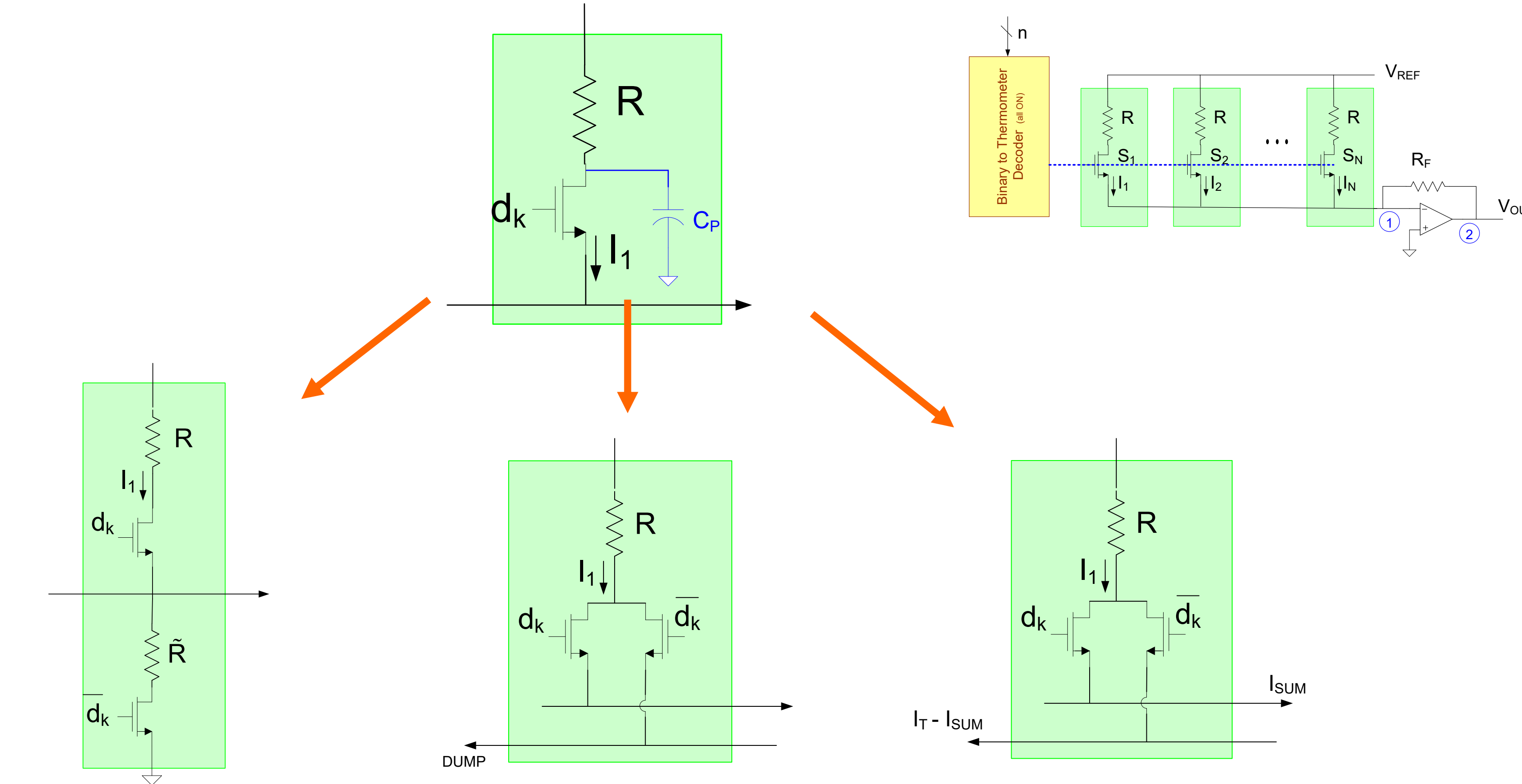
$$|d_{kA}| < |d_k|$$



Differential Output

- Steer current rather than switch current
- Signal swing needs to be just large enough to move current from left side to right side

Current Steering DACs



β Compensation

C_P Compensation

Differential Output (switched or steered)

Will β compensation "half" resistance of cells?

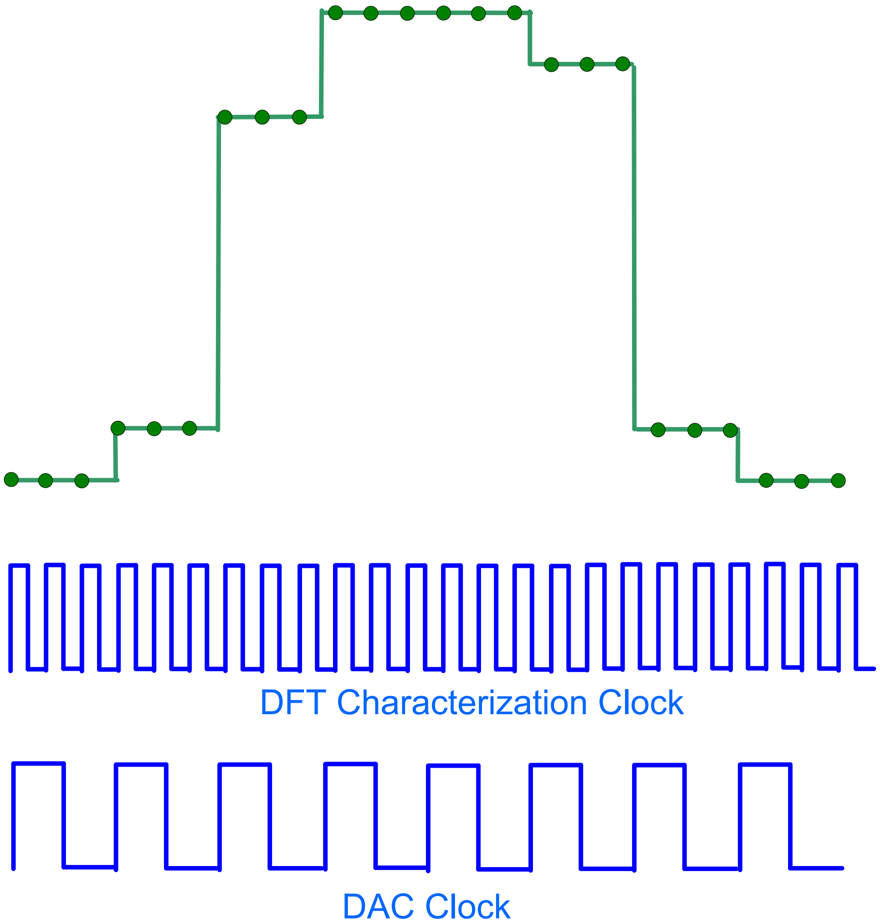
Will β compensation double area for cells?

Is matching of R and compensating R critical?

Can C_p and β compensation be used simultaneously?

Is the frequency-dependent β code dependent?

Spectral Characterization of DACs (a measure of linearity)

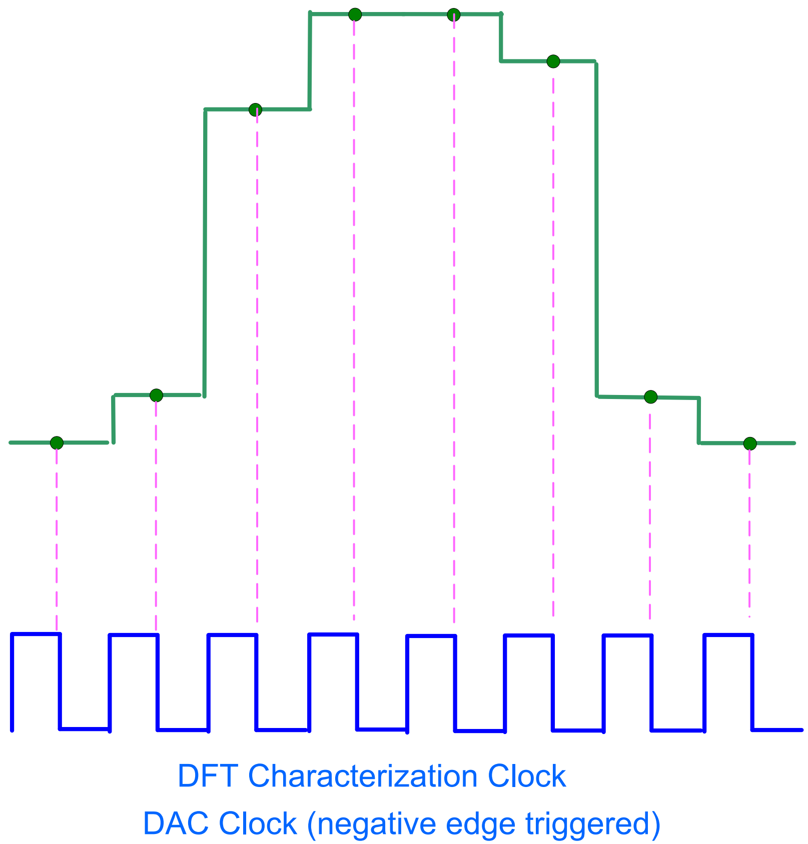


many more samples per DAC clock are often used

(e.g. 64K samples, 31 periods would be approx 2114 samples/period)

Is this how we should characterize the spectral performance of a DAC?

Spectral Characterization of DACs (a measure of linearity)

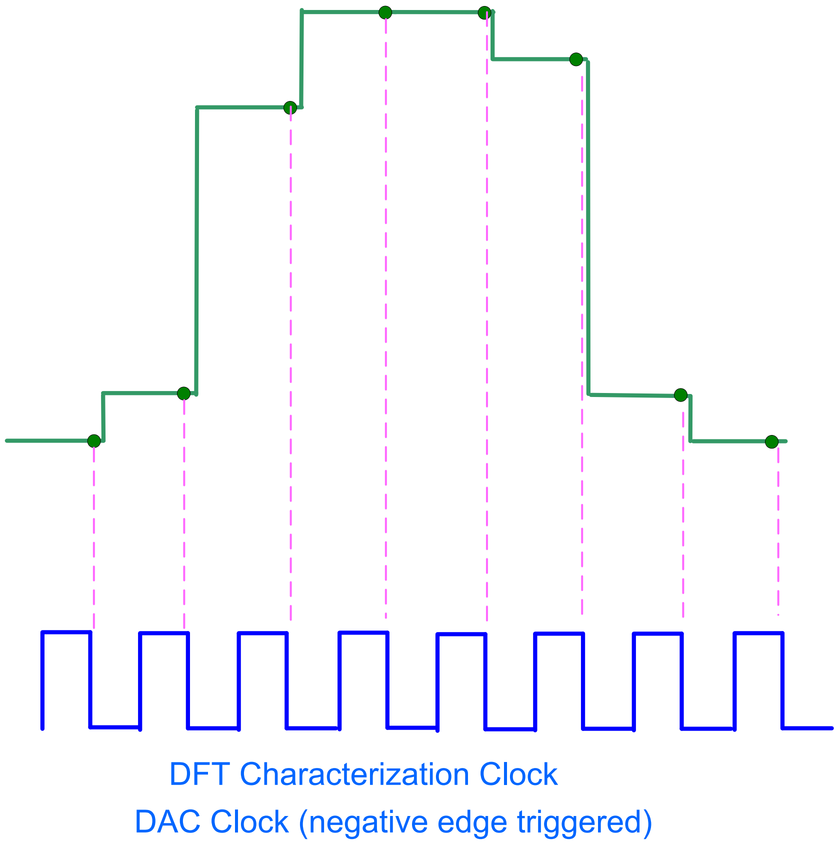


one mid-period sample per DAC clock period (or maybe even less)

Assume Nyquist sampling rate is satisfied

Is this how we should characterize the spectral performance of a DAC?

Spectral Characterization of DACs (a measure of linearity)

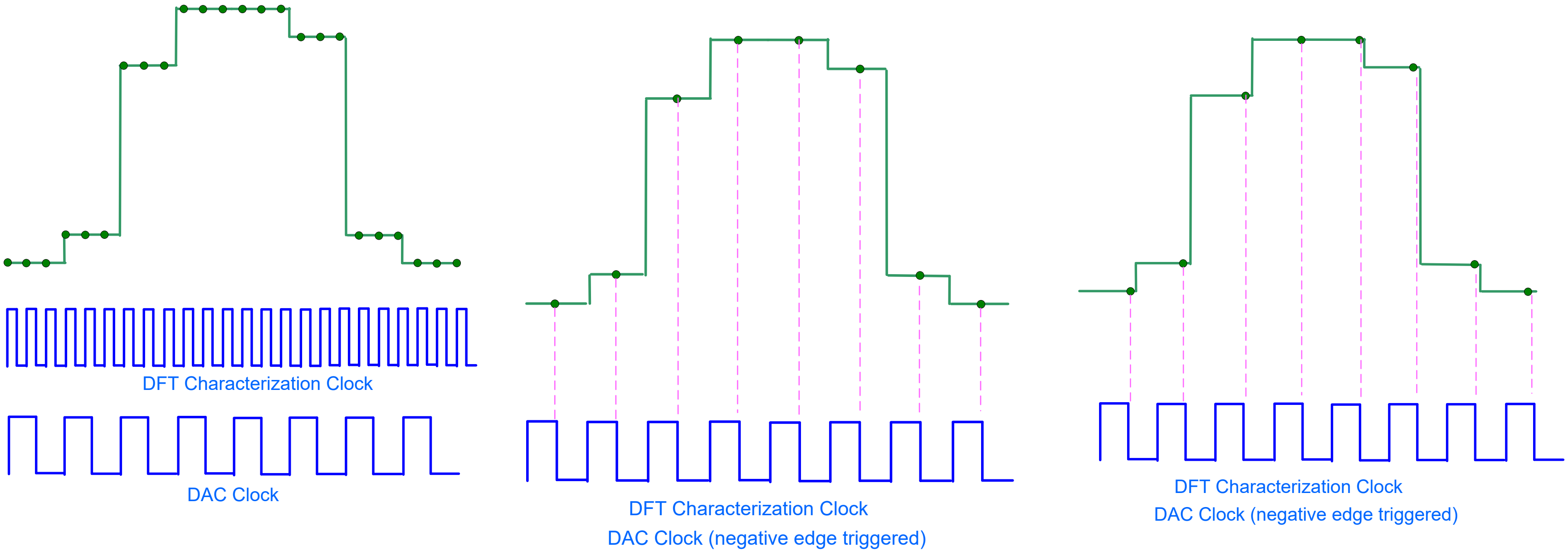


one near-end sample per DAC clock period

Assume Nyquist sampling rate is satisfied

Is this how we should characterize the spectral performance of a DAC?

Spectral Characterization of DACs (a measure of linearity)



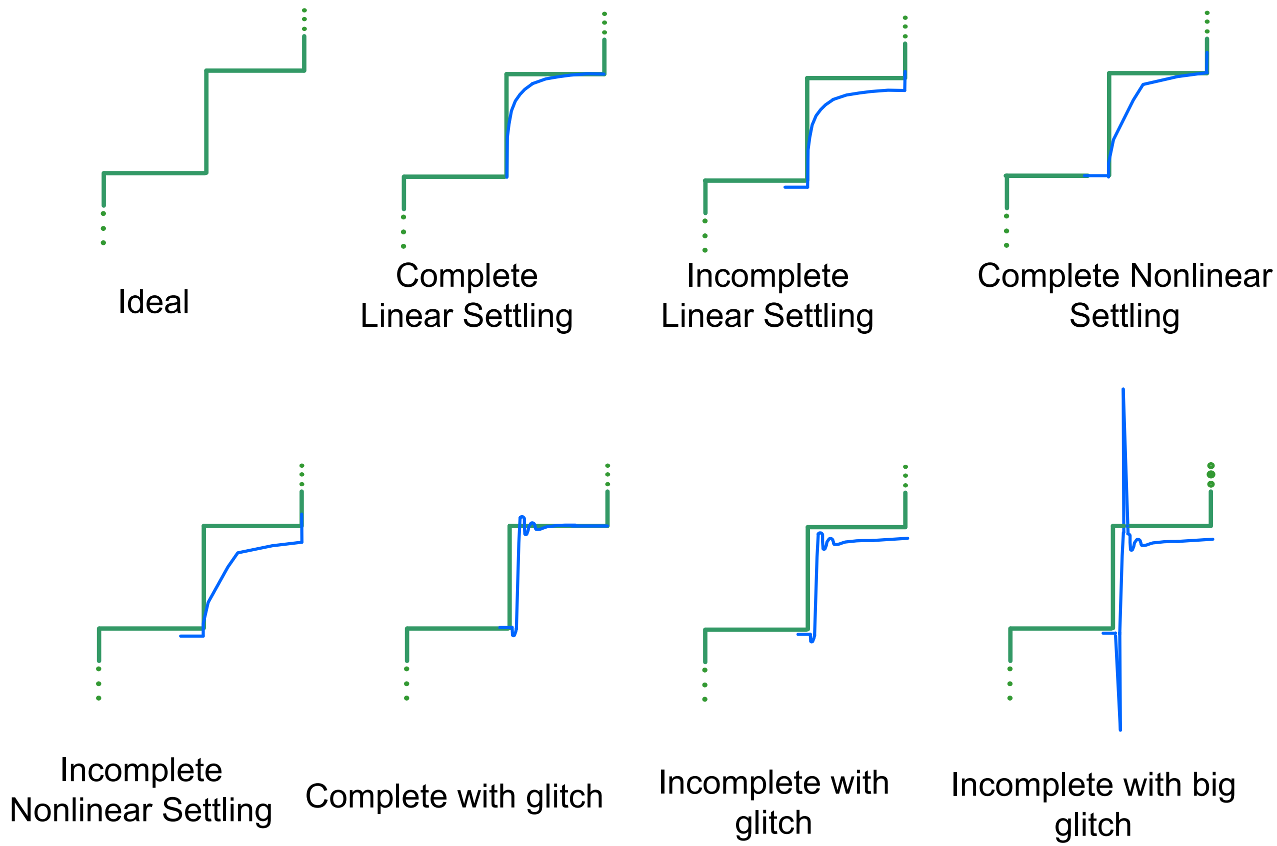
Assume Nyquist sampling rate is satisfied

Does it make a difference?

Yes ! But depends on application which is useful

Spectral Characterization of DACs (a measure of linearity)

Does it make a difference?

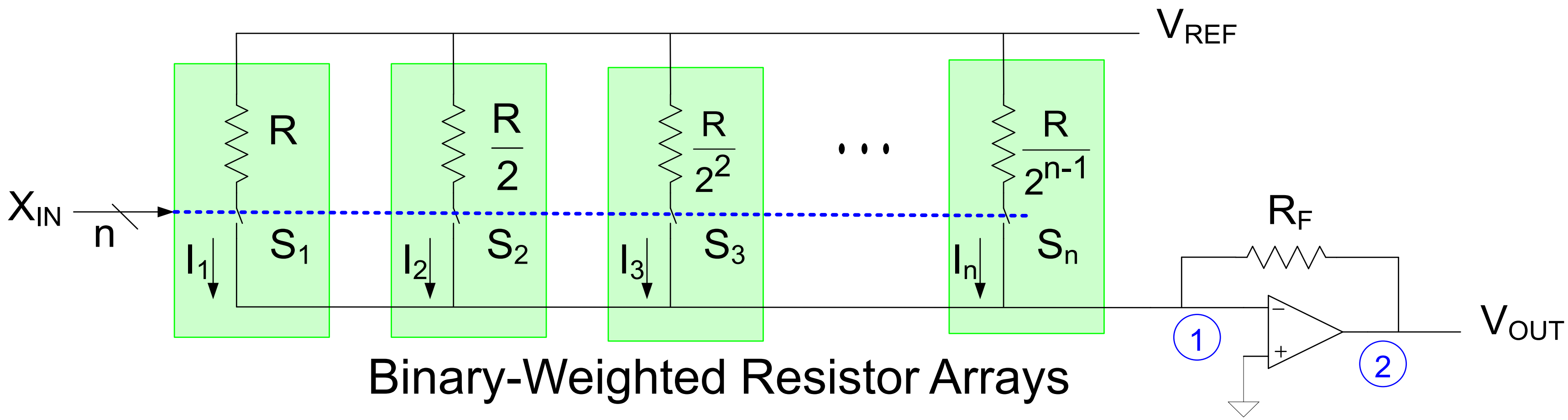


Yes ! But depends on application which is useful

- If entire DAC output is of interest, any nonlinearity including previous code dependence will degrade linearity
- If DAC output is simply sampled, only value at sample point is of concern

Current Steering DACs

Current Steering



Binary-Weighted Resistor Arrays

- Unary cells bundled to implement binary cells (so no net change in number of cells)
- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical
- Large total resistance

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

Large DNL dominantly occurs at mid-code and due to ALL resistors switching together

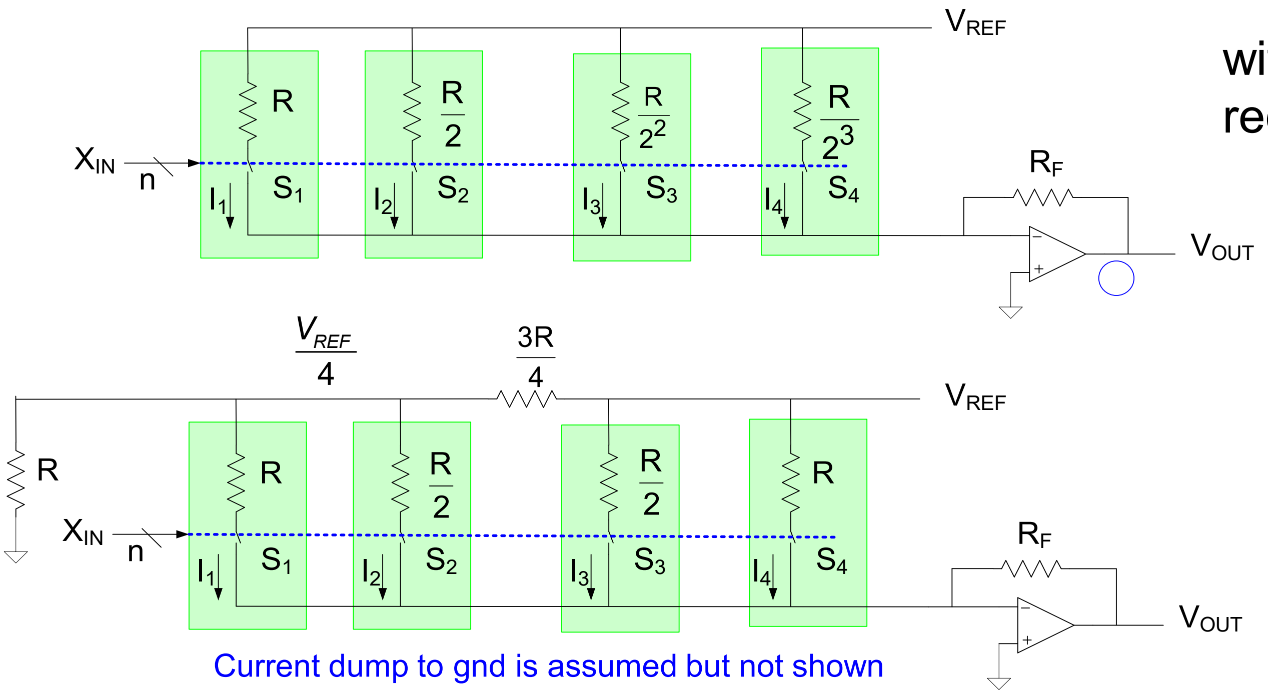
Can unary cell bundling be regrouped to reduce DNL

Current Steering DACs

Reduced Resistance Structure

(actually concerned about number of unary cells, not total ohmic resistance)

with unary R cells, require 2^n-1 cells

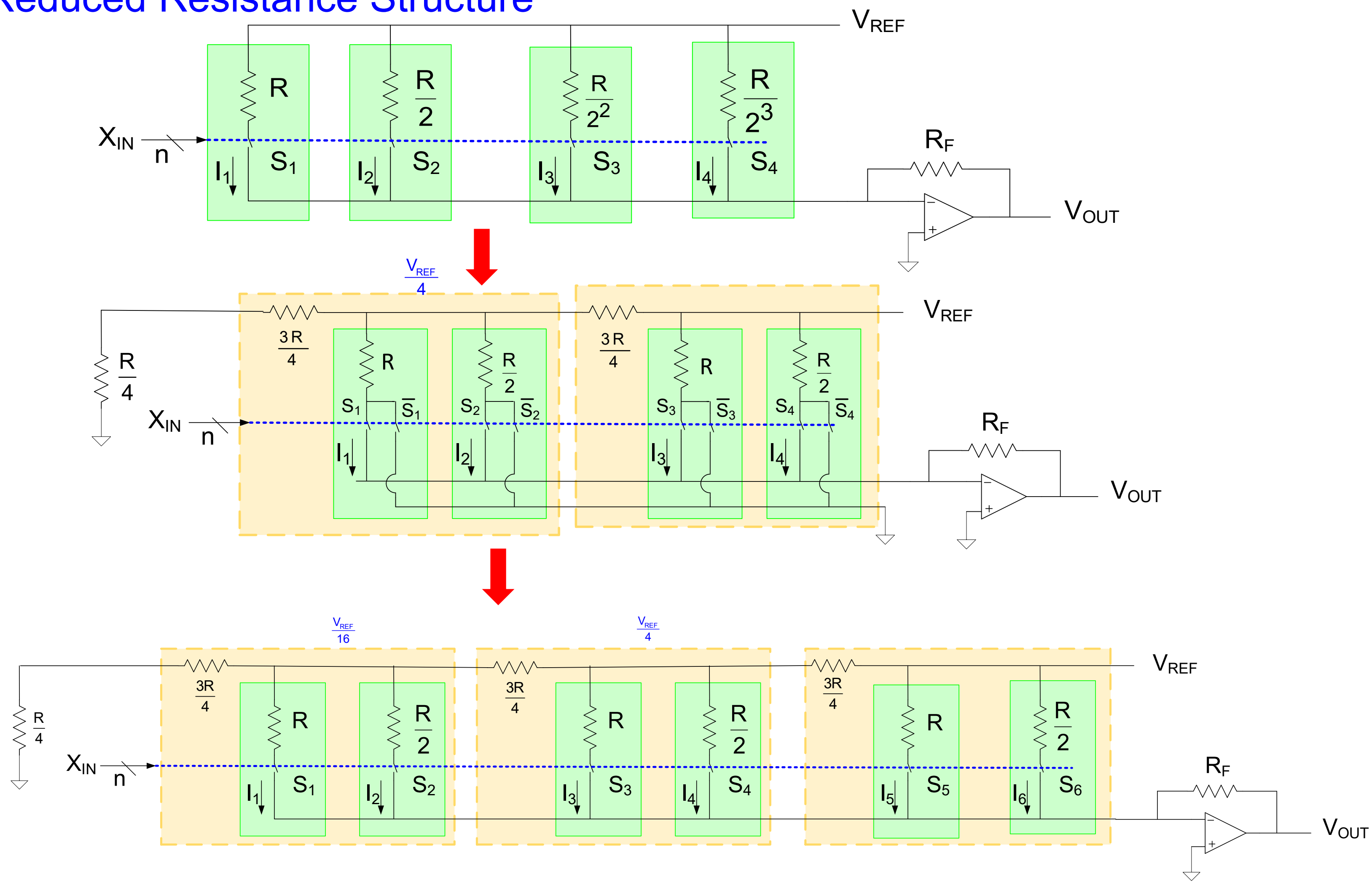


Current dump to gnd is assumed but not shown

- Significant reduction in resistance possible
- Can be inserted at more than one place to further reduce resistance values
- Introduces a “floating node” but voltage on floating node does not change (if current is stee
- Current drawn from V_{REF} does not change with code
- Dummy switching can be used for β compensation
- If inserted at each intersection becomes R-2R structure

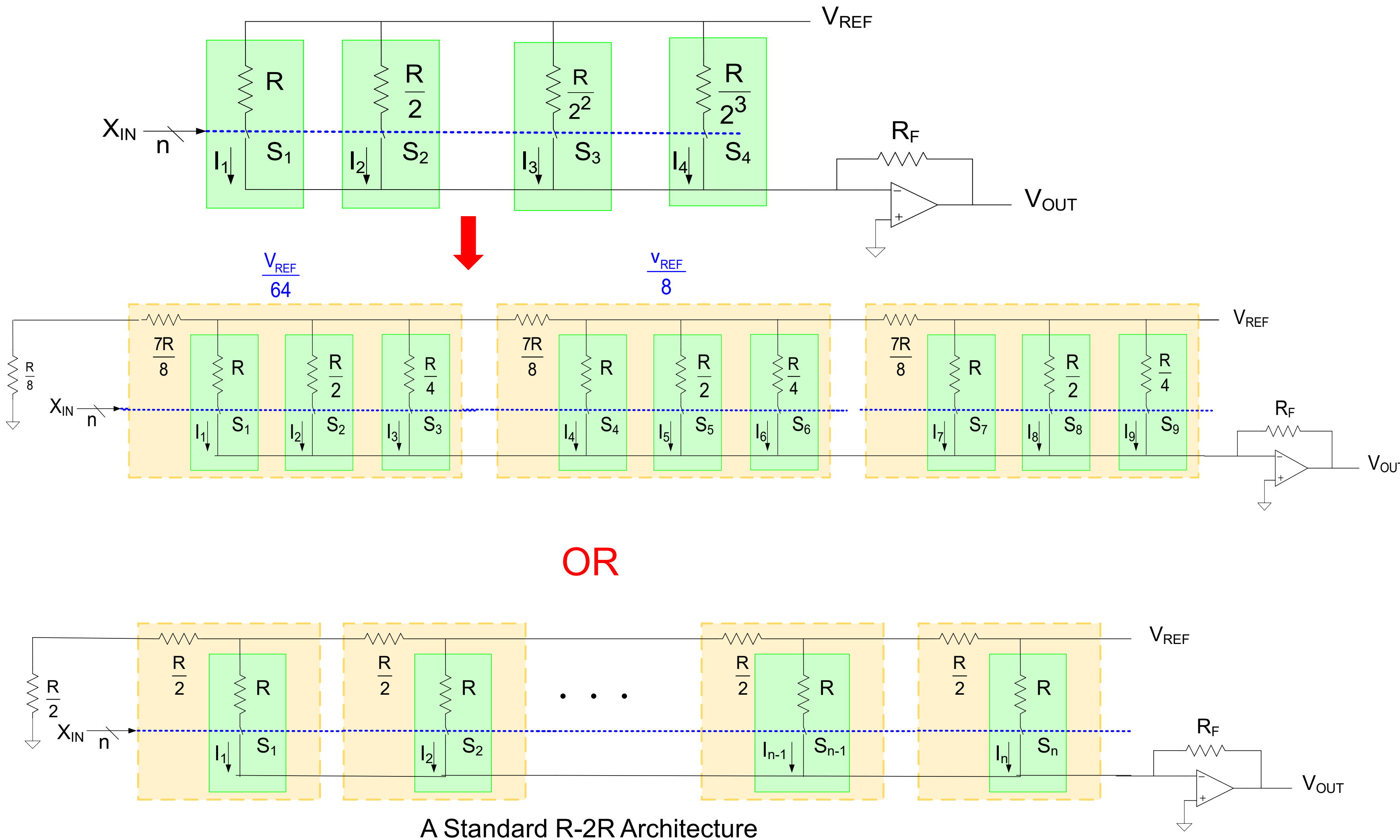
Current Steering DACs

Reduced Resistance Structure



Current Steering DACs

Reduced Resistance Structure

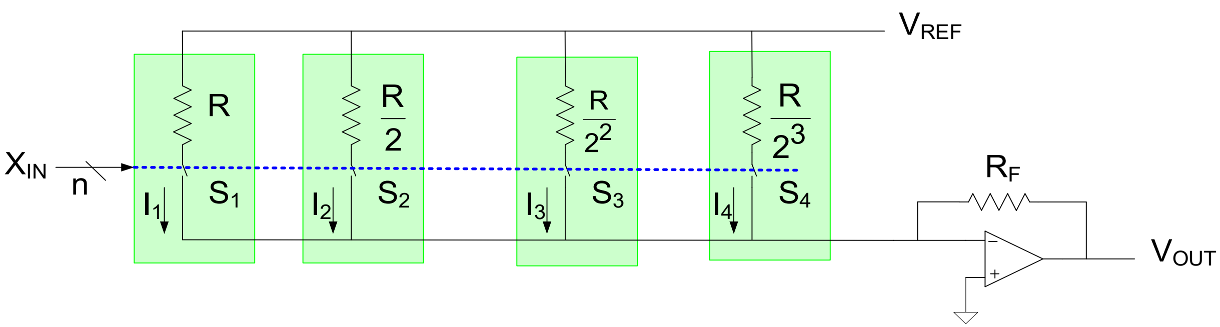


A Standard R-2R Architecture

with unary R/2 cells, required 3n+1 cells compared to 2^n-1 cells for binary bundled array

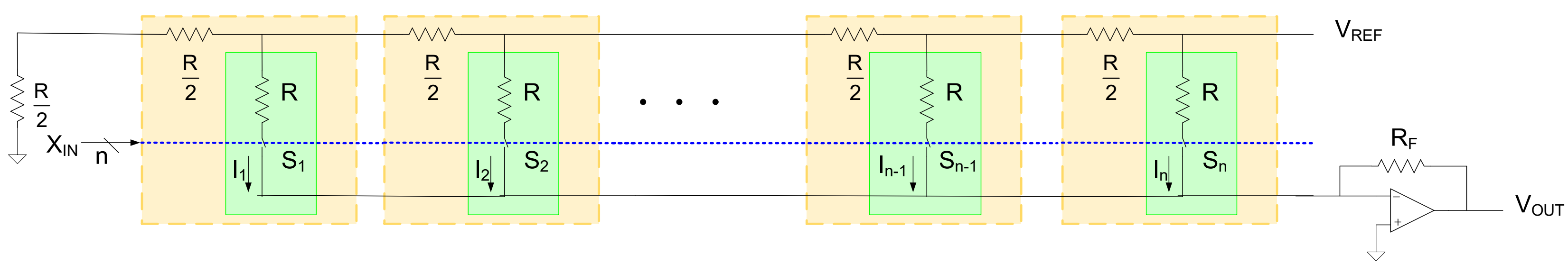
Current Steering DACs

Reduced Resistance Structure



2^n-1 cells

3n+1 cells

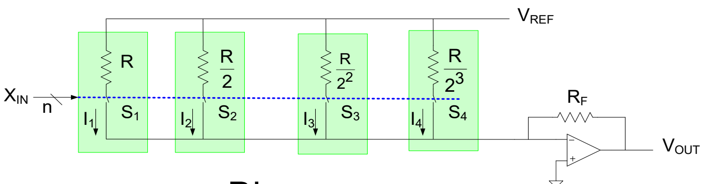


Is the R-2R structure smaller ?
Does the R-2R structure perform better?

What metric should be used for comparing performance?

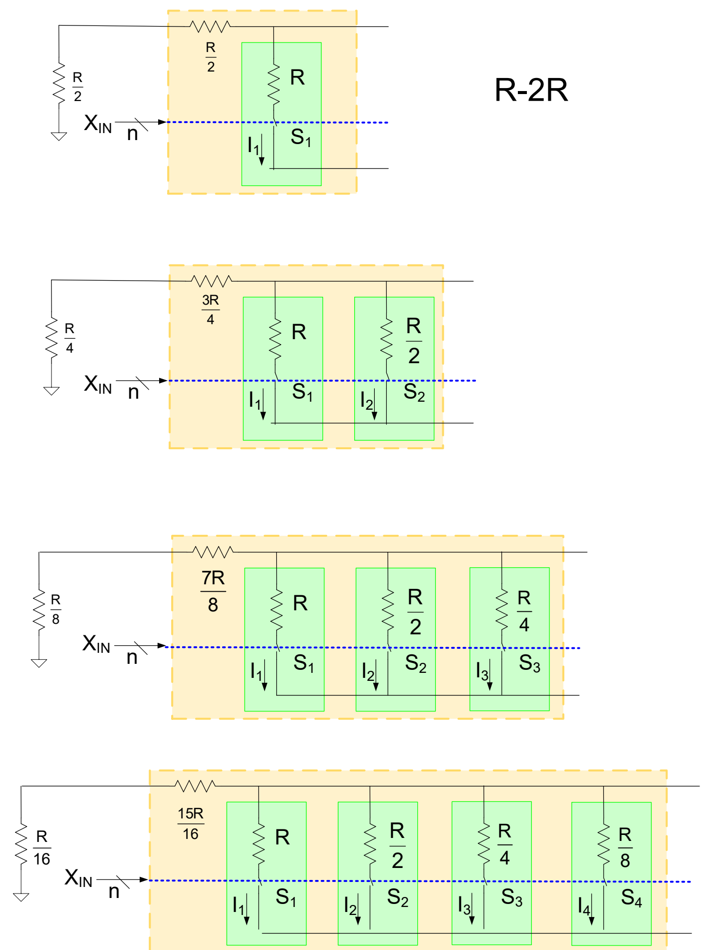
Current Steering DACs

Reduced Resistance Structure

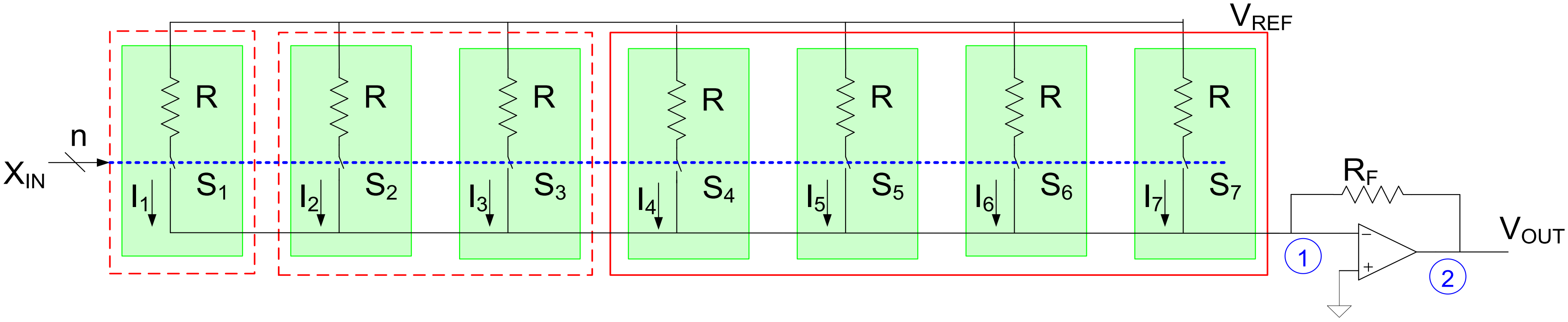


Binary

Slice Grouping Options with Series Resistors



Current Steering DACs



Binary-Weighted Resistor Arrays

Actual layout of resistors is very important

Performance of Thermometer Coded vs Binary Coded DACs

Conventional Wisdom:

- Thermometer-coded structures have inherently small DNL
- Binary coded structures can have large DNL
- INL of both structures is comparable for same total area (provided area appropriately allocated)

Comparison of Thermometer Coded and Binary Coded DACs

- Will consider String DAC but nearly same results for current-steering DACs
- Current Steering DAC will generate current from resistors
- For Binary Coded DAC, MSB: 2^{n-1} unary cells in parallel …. LSB: single unary cell

- Consider unit resistor of area $2\mu m^2$ (shape not critical)
- Matching parameter A_R=0.02µm
- R_N=1K (not critical)

$$\sigma_R = \frac{R_N}{\sqrt{A}} A_{\rho R}$$

- Assume Gaussian Distribution of Resistors

File: BinaryWeightedDACInl.m

Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

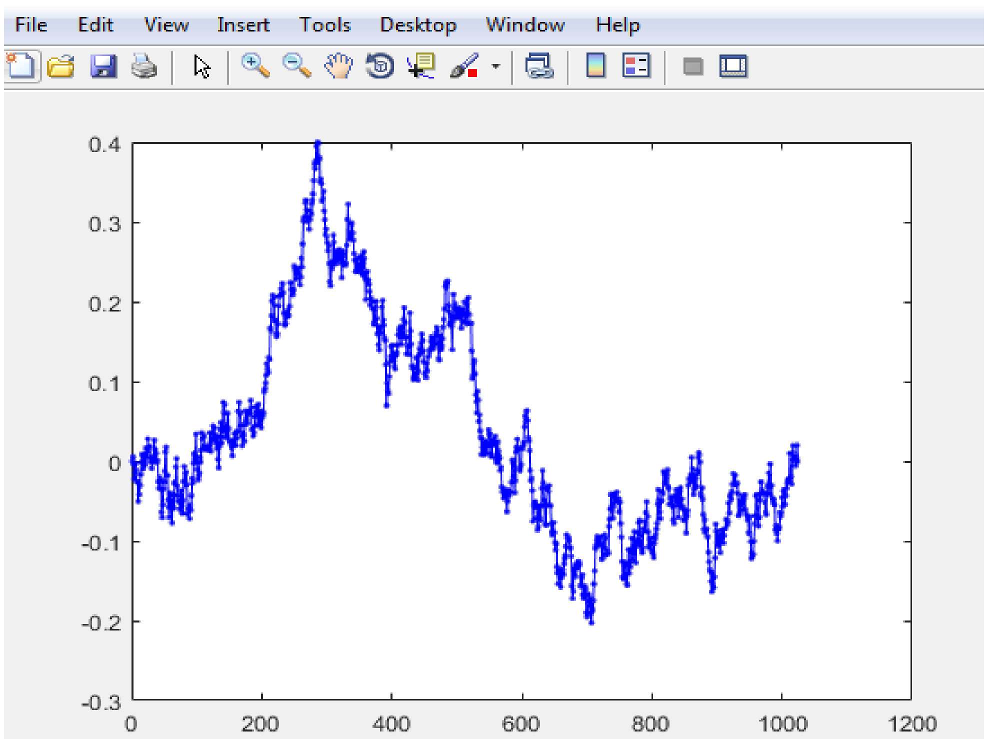
String DAC

A_R=0.02μm

R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 1: INL_k



Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

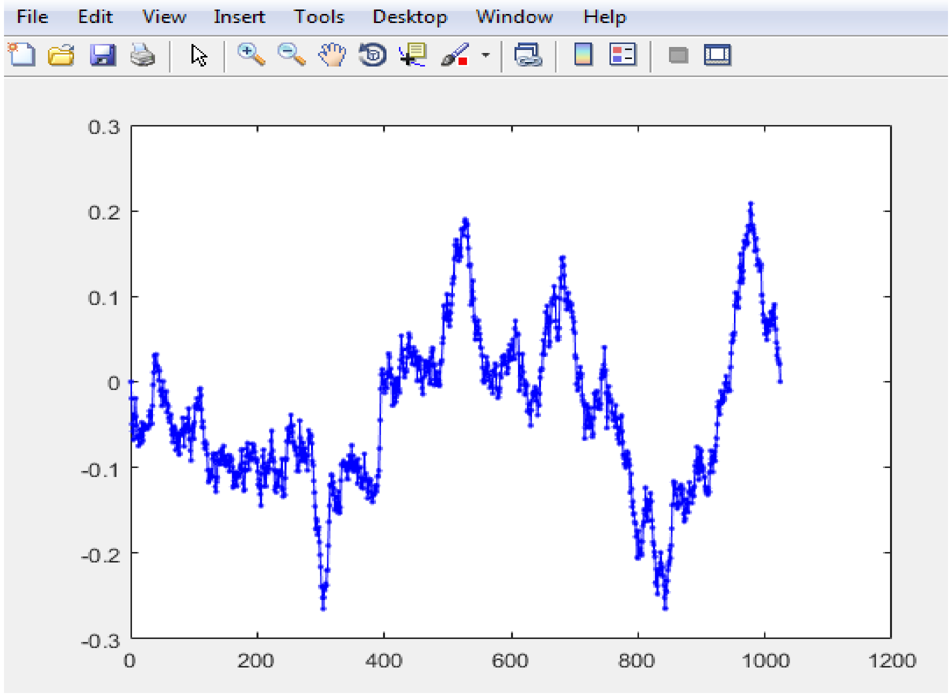
String DAC

A_R=0.02µm

R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 2: INL_k



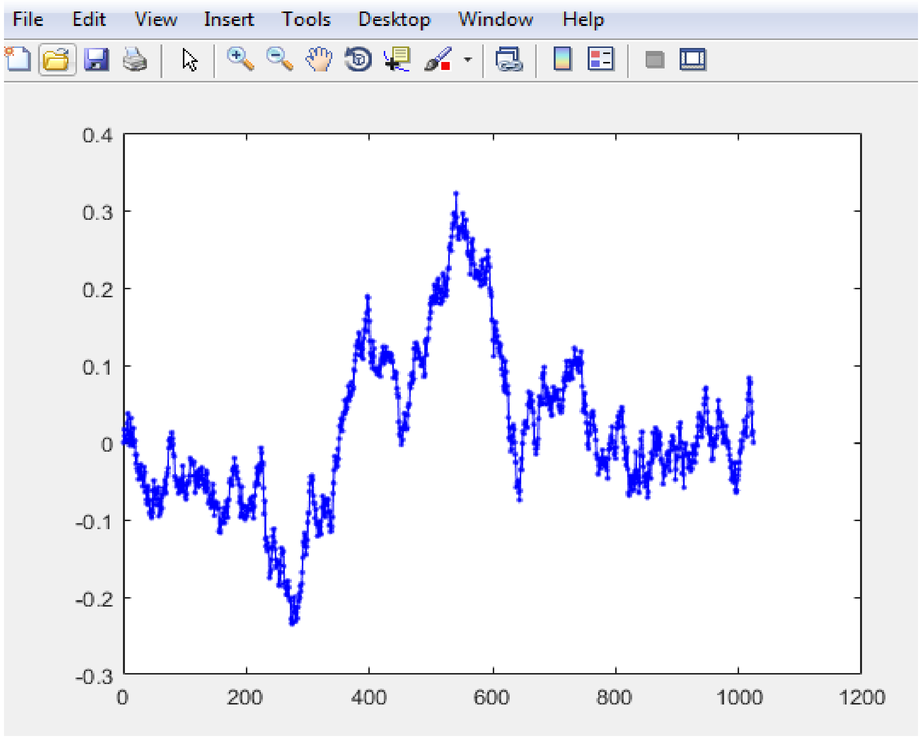
Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

String DAC

→ A_R=0.02μm, R_N=1K → Resistor Sigma= 14.14 Ω

Simulation 3: INL_k



Comparison of Thermometer Coded and Binary Coded DACs

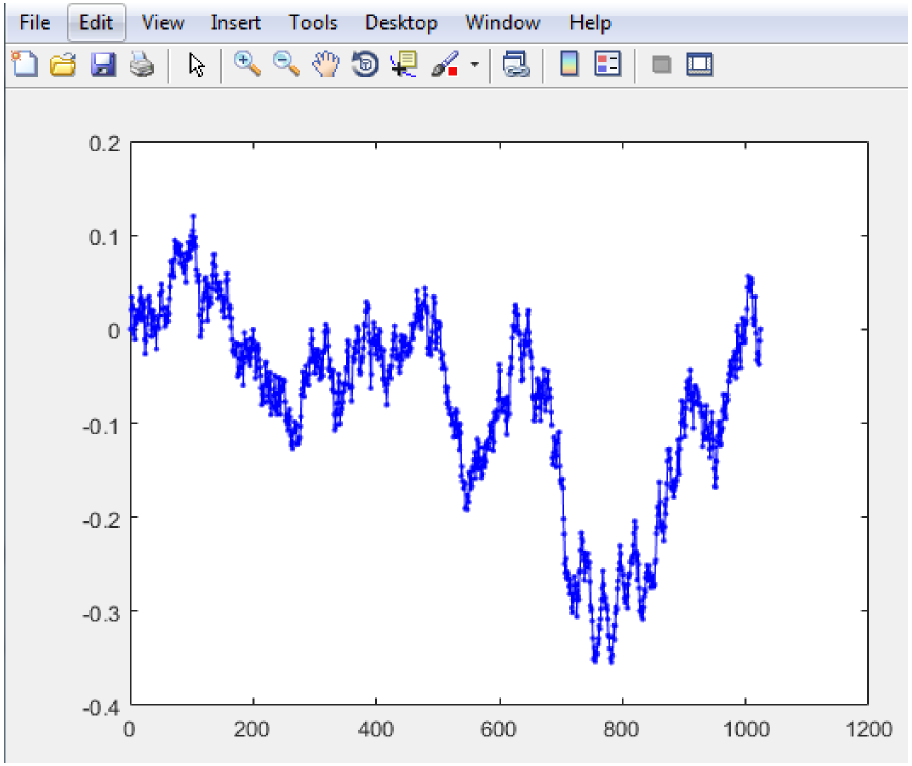
Example: n=10

String DAC

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 4: INL_k



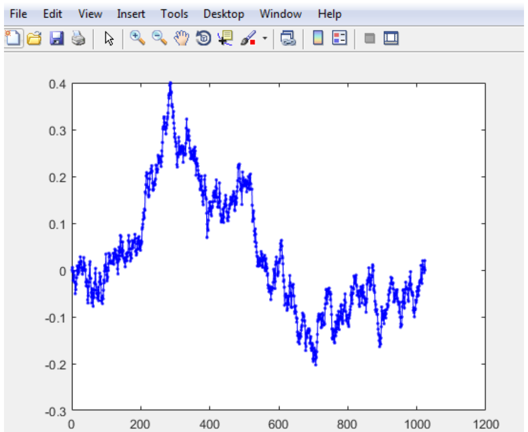
Comparison of Thermometer Coded and Binary Coded DACs

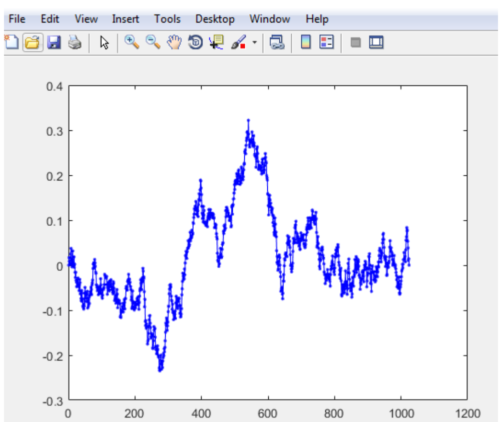
Example: n=10

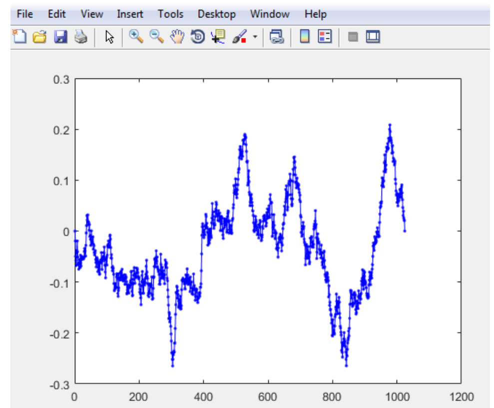
String DAC

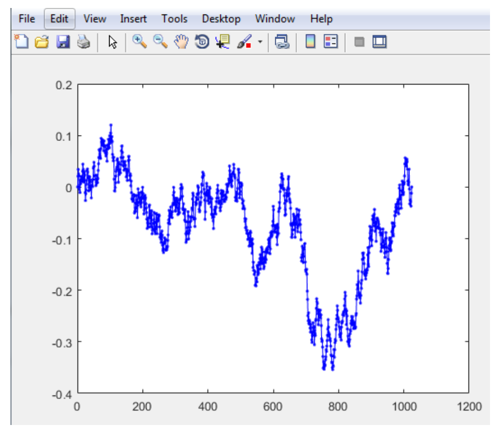
A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω









Low DNL and random walk nature should be apparent

Comparison of Thermometer Coded and Binary Coded DACs

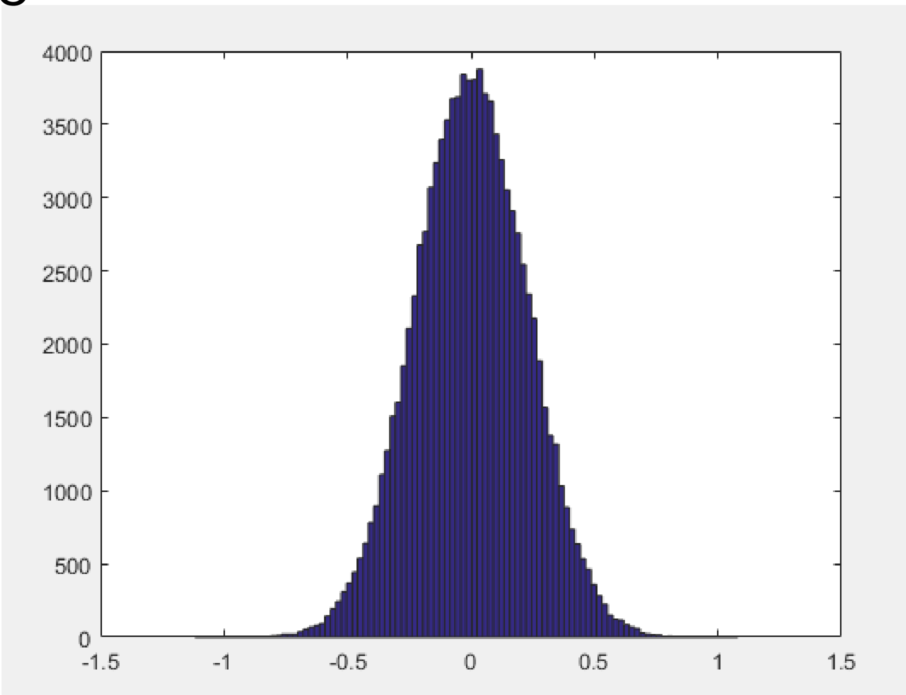
Example: n=10

String DAC

A_R=0.02µm

R_N=1K

Resistor Sigma= 14.14 Ω



INLkmax_mean = -2.11116e-05

INLkmax_sigma = 0.226783

Histogram of INL_{kmax} from 100,000 runs

Appears to be Gaussian

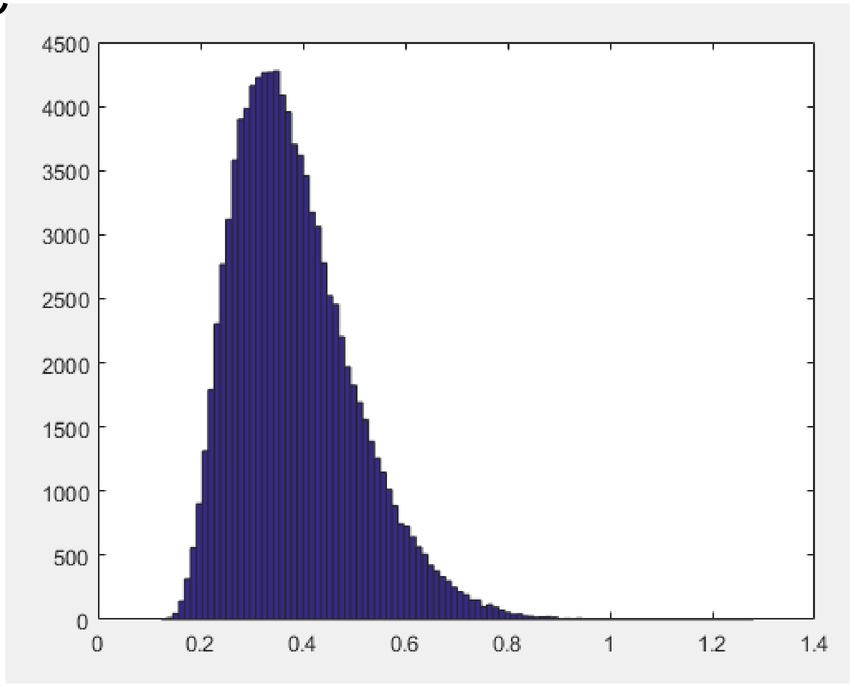
Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

String DAC

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω



INLmean = 0.384382
INLsigma = 0.117732

Histogram of INL from 100,000 runs

Not Gaussian

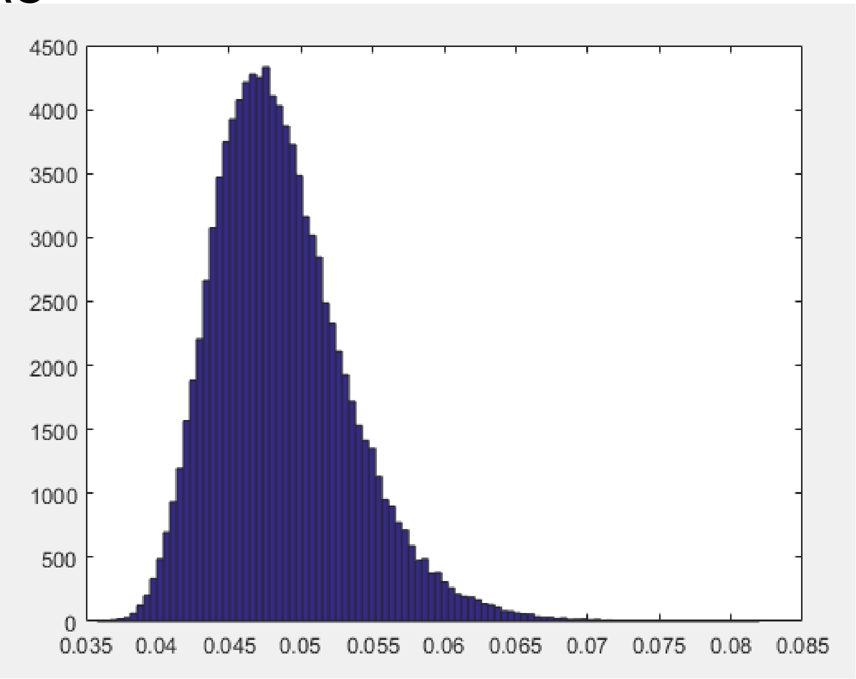
Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

String DAC

A_R=0.02µm
R_N=1K

Resistor Sigma= 14.14 Ω



DNLmean = 0.0486494
DNLsigma = 0.00471025

Histogram of DNL from 100,000 runs

Not Gaussian but both mean and sigma are very small

Comparison of Thermometer Coded and Binary Coded DACs

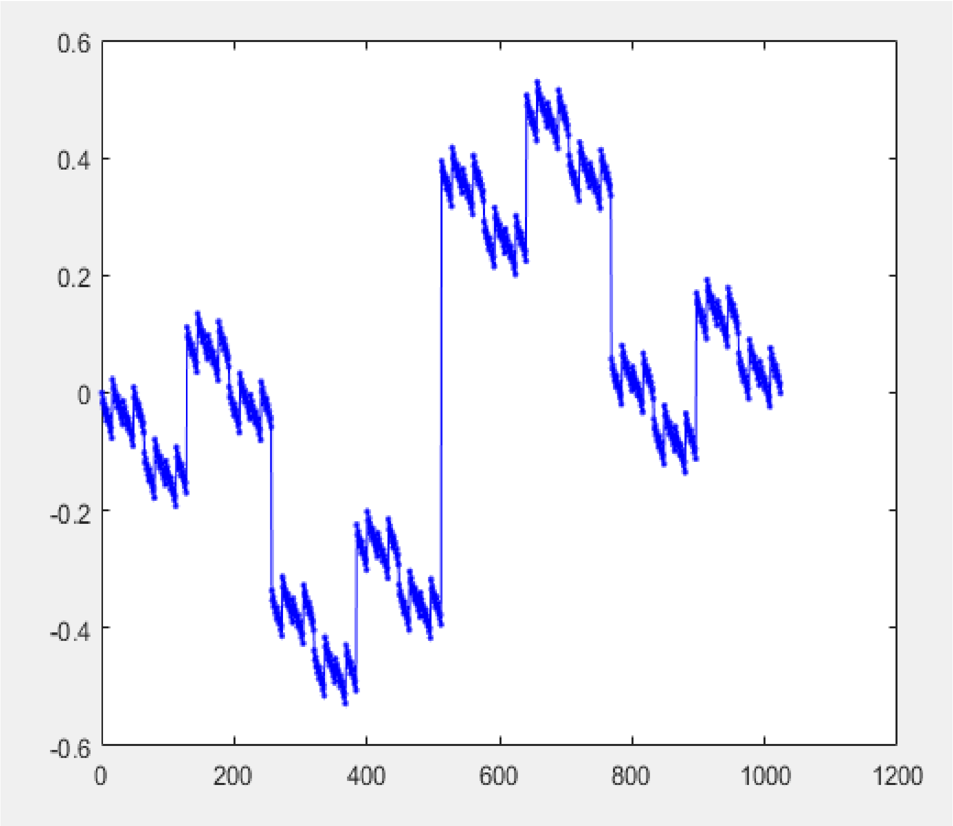
Example: n=10

Binary DAC

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 1: INL_k



Comparison of Thermometer Coded and Binary Coded DACs

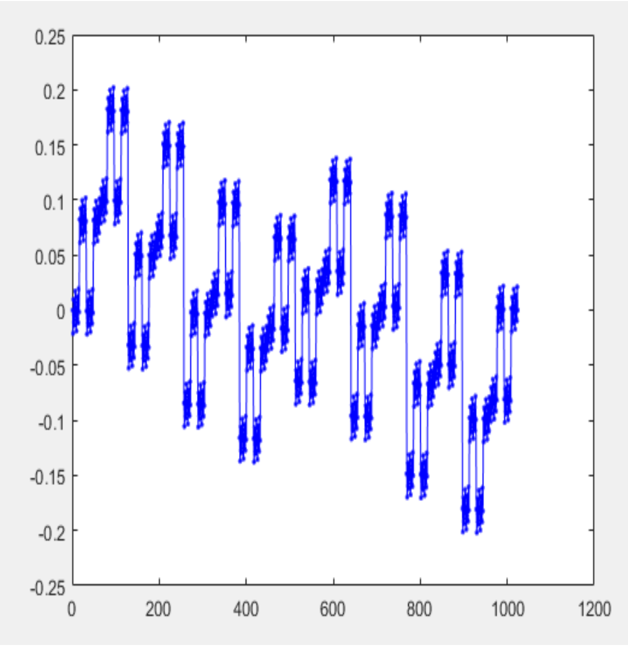
Example: n=10

Binary DAC

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 2: INL_k



Comparison of Thermometer Coded and Binary Coded DACs

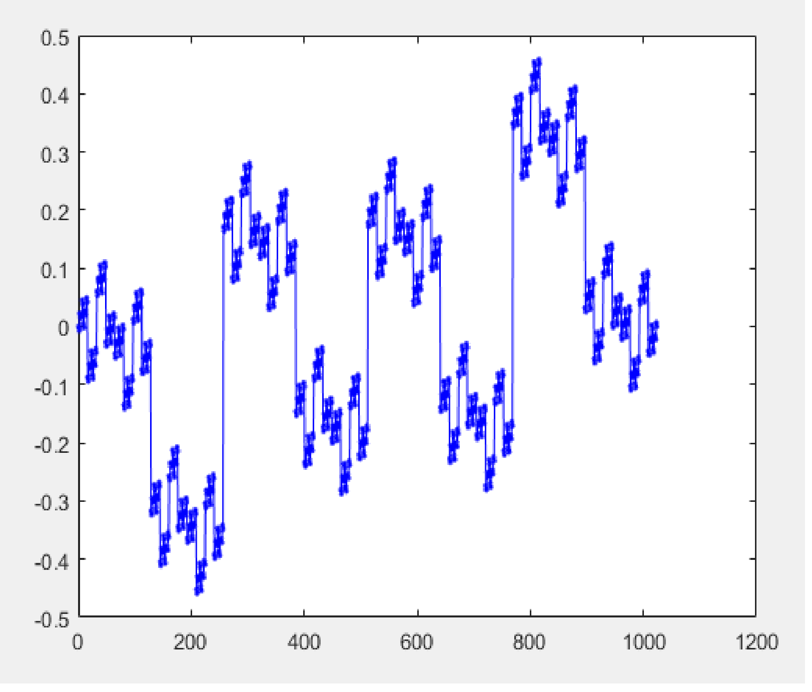
Example: n=10

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Binary DAC

Simulation 3: INL_k



Comparison of Thermometer Coded and Binary Coded DACs

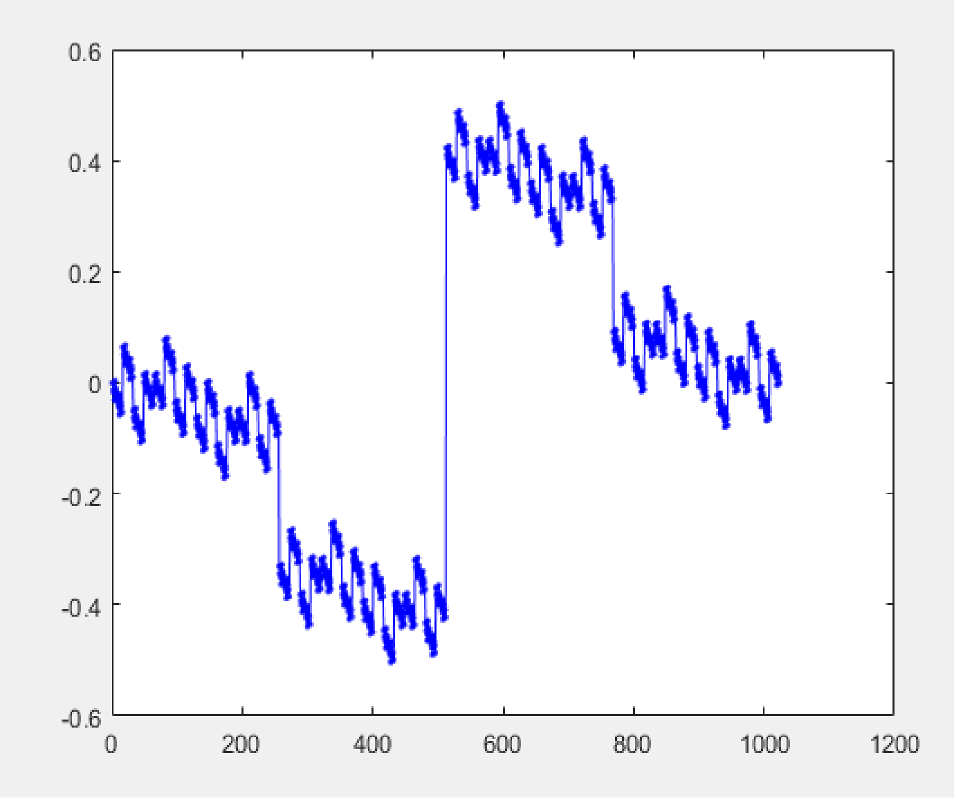
Example: n=10

Binary DAC

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 4: INL_k



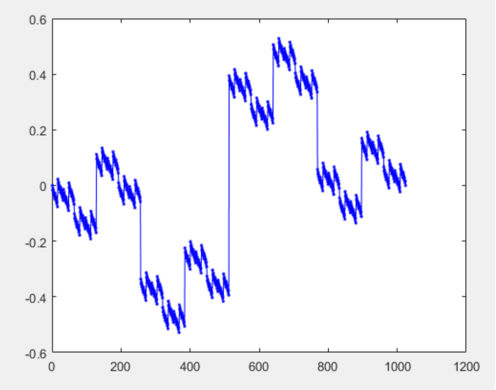
Comparison of Thermometer Coded and Binary Coded DACs

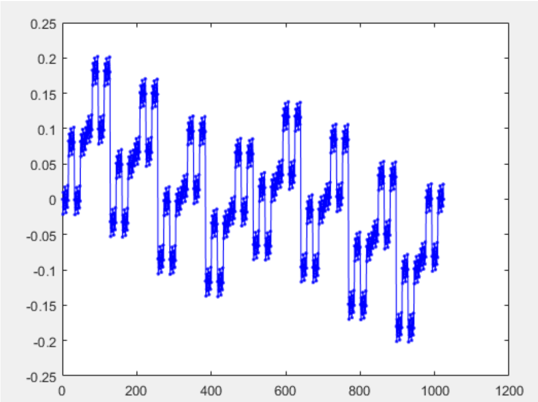
Example: n=10

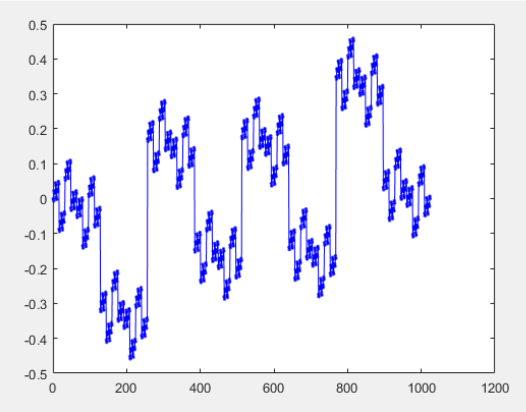
Binary DAC

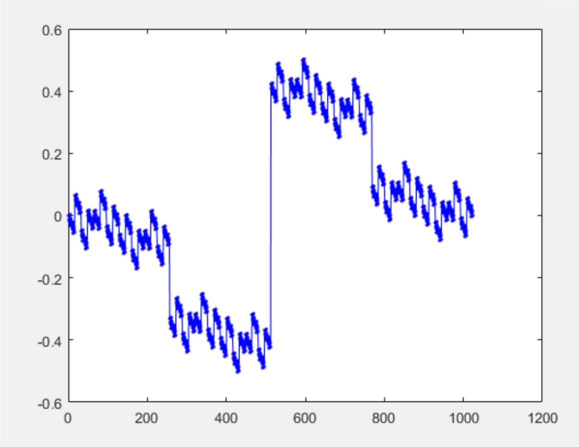
A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω









Large DNL bit INL does not appear to be much different than for string DAC

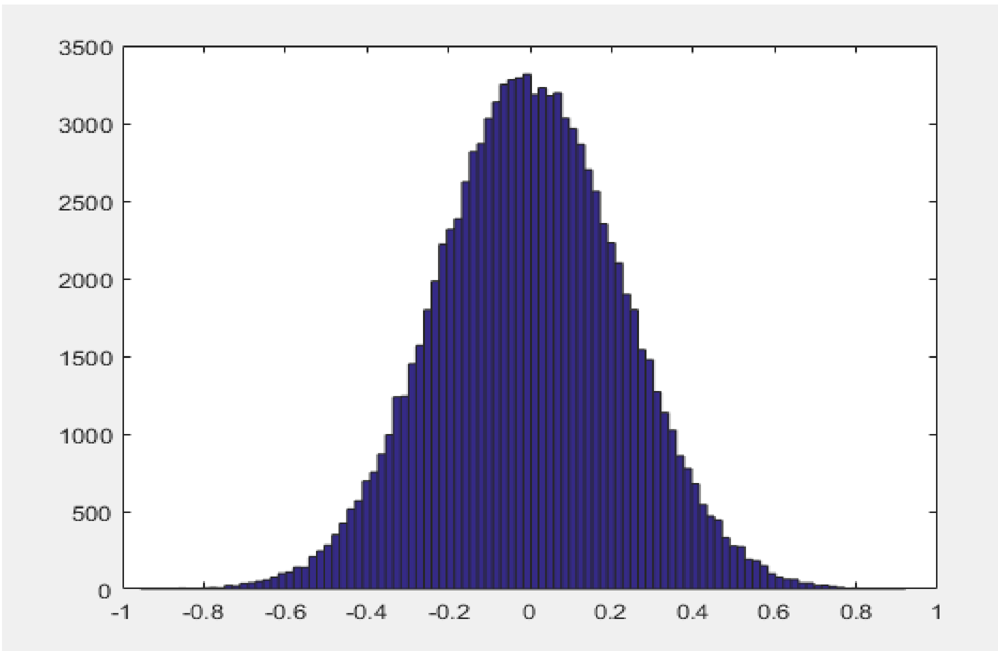
Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Binary DAC



INLkmax_mean = -.00526008
INLkmax_sigma = 0.23196

Histogram of INL_{kmax} from 100,000 runs

Appears to be Gaussian

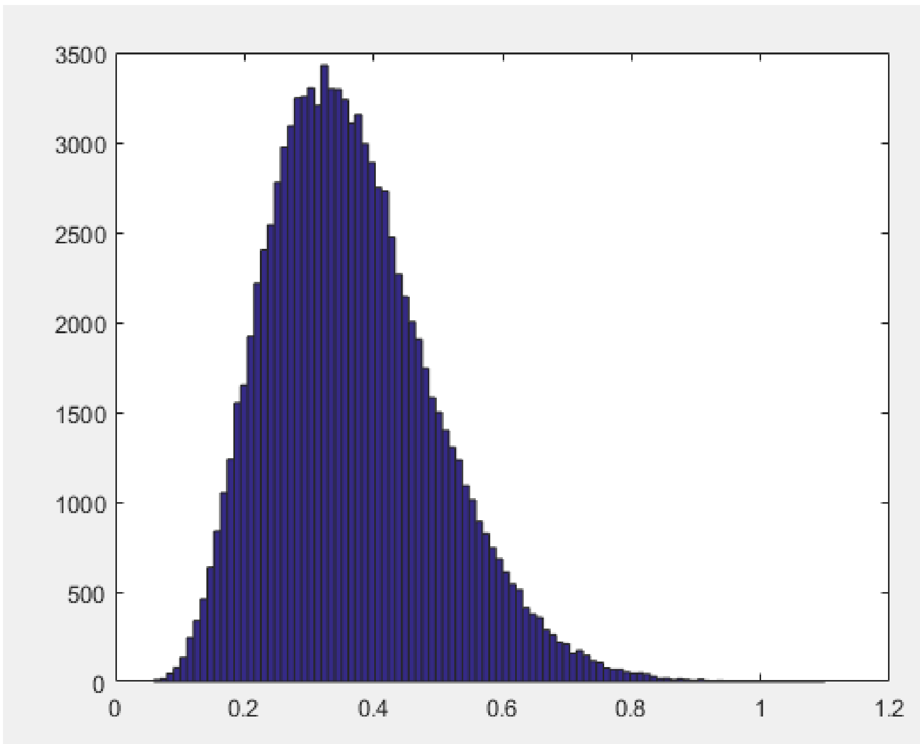
Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

A_R=0.02µm
R_N=1K

Resistor Sigma= 14.14 Ω

Binary DAC



INLmean = 0.368441
INLsigma = 0.126133

Histogram of INL from 100,000 runs

Not Gaussian

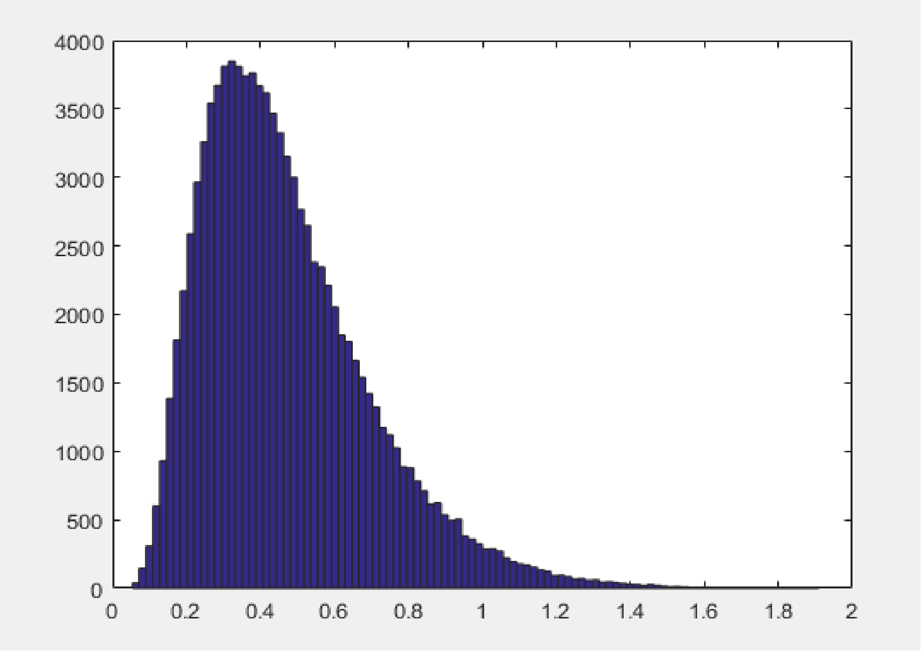
Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

Binary DAC

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω



DNLmean = 0.46978
DNLsigma = 0.227768

Histogram of DNL from 100,000 runs

Not Gaussian and both mean and sigma are not small

Comparison of Thermometer Coded and Binary Coded DACs

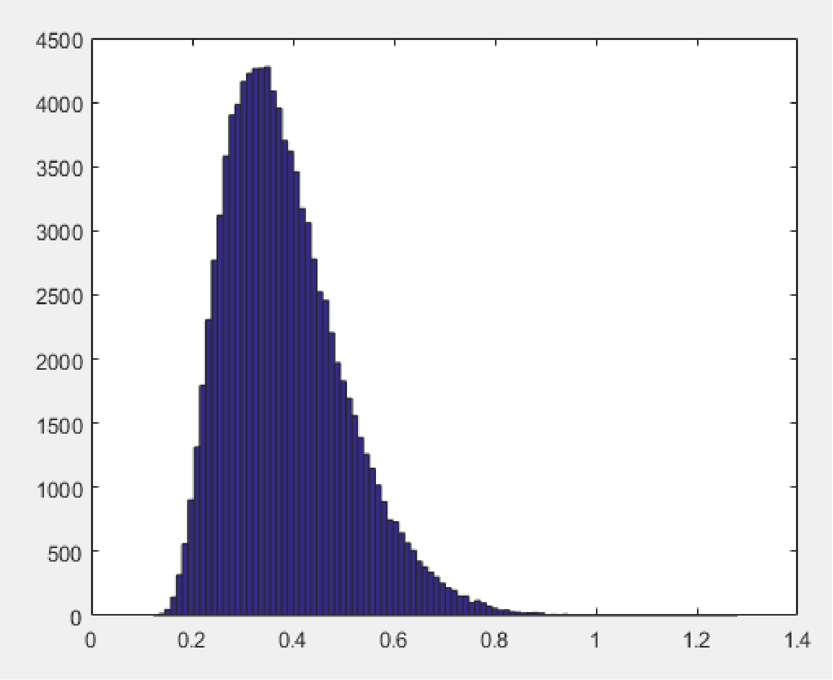
Example: n=10

A_R=0.02μm
R_N=1K

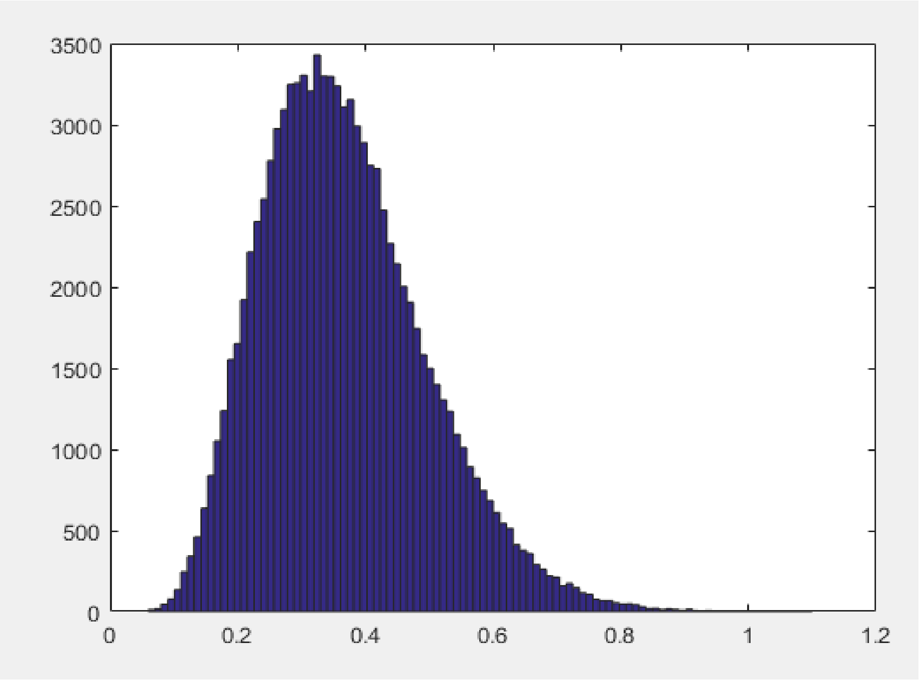
Resistor Sigma= 14.14 Ω

Both structures have essentially the same area

String DAC



Binary DAC



Histogram of INL from 100,000 runs

Since mathematical form for PDF is not available, not easy to analytically calculate yield

Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

A_R=0.02μm
R_N=1K

Resistor Sigma= 14.14 Ω

Both structures have essentially the same area

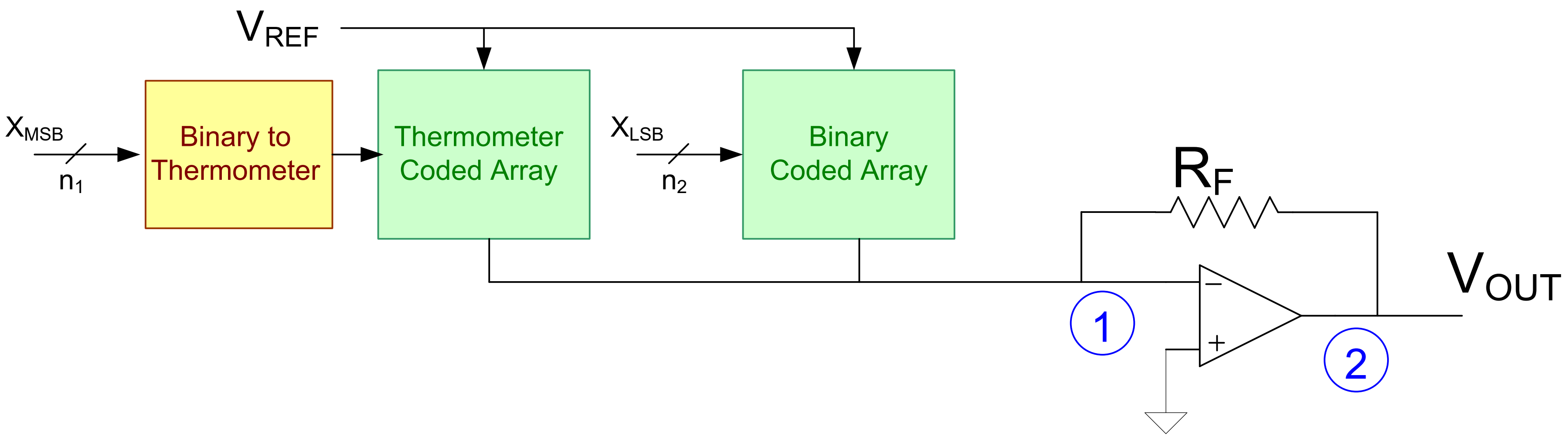
String DAC

Resolution = 10   AR = 0.02   Nruns = 100000
Rnom = 1000   Area Unit Resistor = 2μm^2 Resistor Sigma= 14.1421
INLkmax_mean = -2.11116e-05   INLkmax_sigma = 0.226783
INLmean = 0.384382   INLsigma = 0.117732
INLtarget = 0.5000   Yield(%) = 84.0120

Binary DAC

Resolution = 10   AR = 0.02   Nruns = 100,000
Rnom = 1000   Area unit resistor=2μm^2 Resistor Sigma= 14.1421
INLmean = 0.367036   INLsigma = 0.128294
INLkmax_mean = 0.000130823   INLkmax_sigma = 0.226276
DNLmean = 0.46978   DNLsigma = 0.227768
INLtarget = 0.5000   Yield (%) = 84.8580

Current Steering DACs



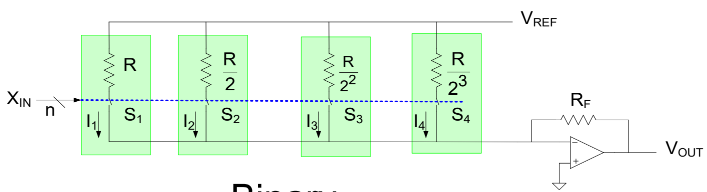
Segmented Resistor Arrays

- Combines two types of architectures
- Can inherit advantages of both thermometer and binary approach
- Minimizes limitations of both thermometer and binary approach

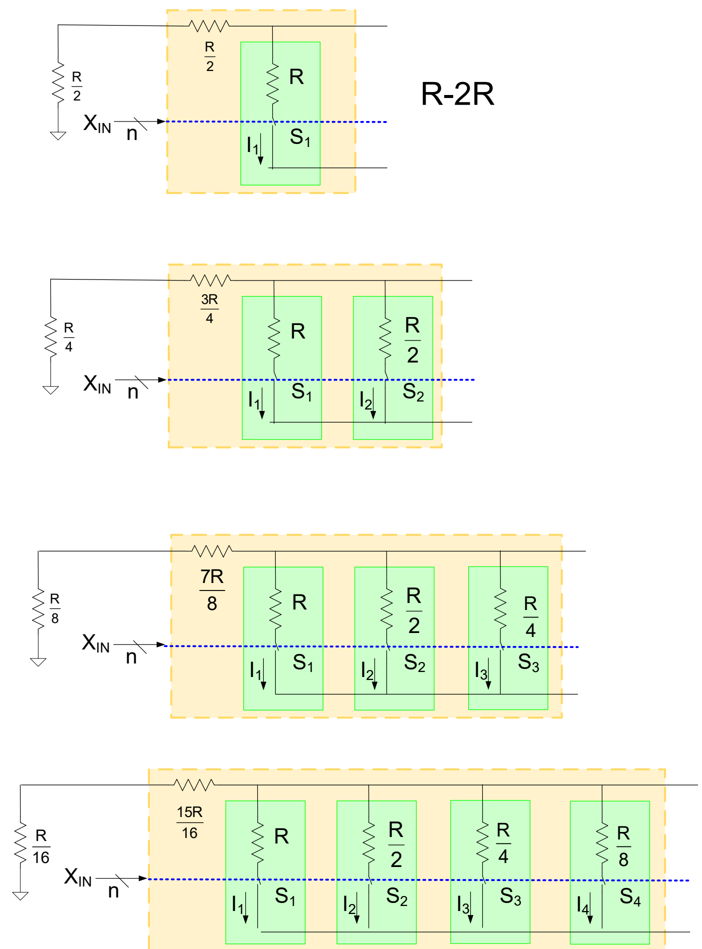
Current Steering DACs

Reduced Resistance Structure

Slice Grouping Options with Series Resistors



Binary



Is it better to use series unary cells to form R or parallel unary cells to form $\frac{R}{2^n}$?

In the two scenarios, is the dominant area allocated to the MSB or the LSB part of the ladder?

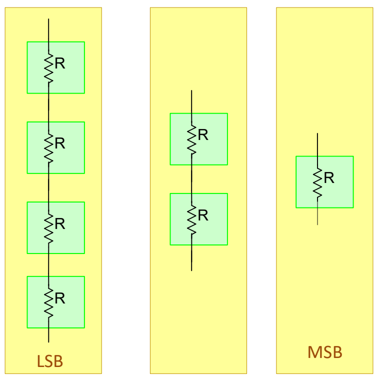
Will this choice make much difference in yield?

What yield-related performance metric will be most affected?

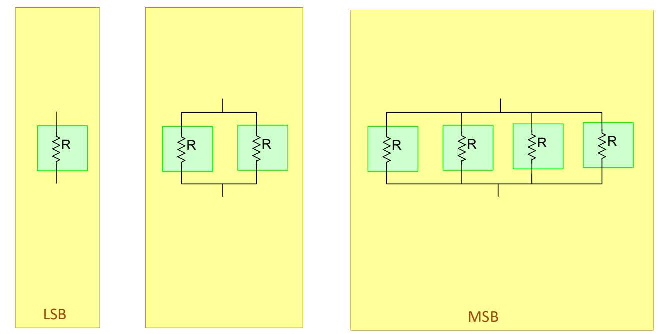
Current Steering DACs

Reduced Resistance Structure

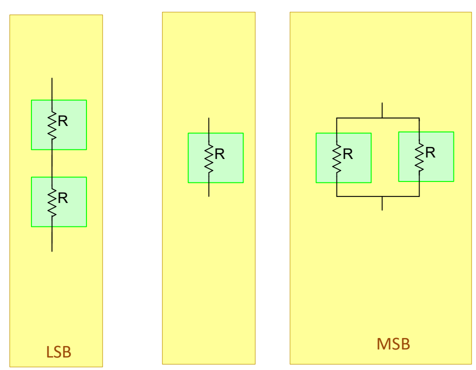
Is it better to use series unary cells to form R or parallel unary cells to form $\frac{R}{2^n}$?



2^n-1 cells



2^n-1 cells



for n odd $2^{\frac{n+3}{2}} - 3$ cells

n		Series	Parallel	Split
3		7	7	5
5		31	31	13
7		127	127	29
9		511	511	61
11		2047	2047	125
13		8191	8191	253
15		32767	32767	509

Comparison of Thermometer Coded and Binary Coded DACs

Example: n=10

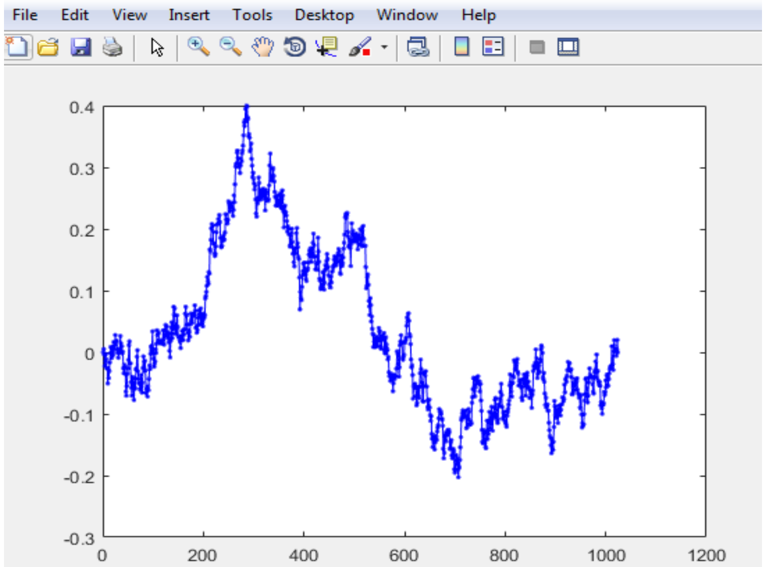
String DAC

A_R=0.02μm

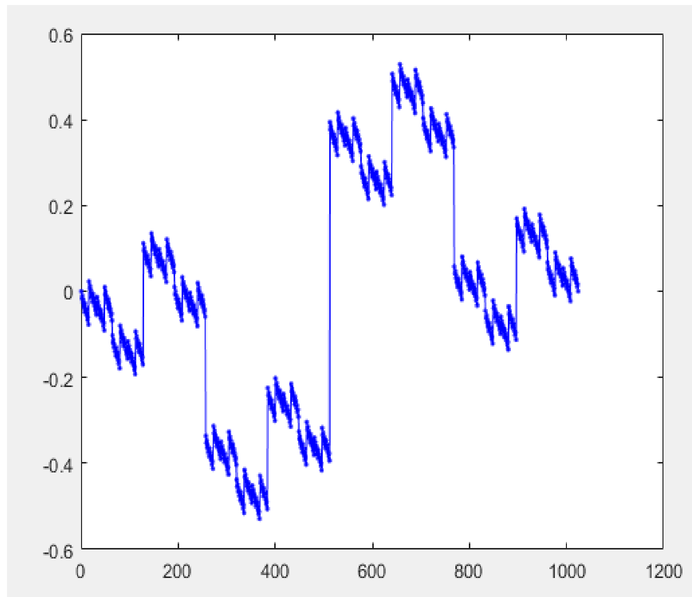
R_N=1K

Resistor Sigma= 14.14 Ω

Simulation 1: INL_k



String



Binary Weighted

Actual outputs will differ significantly

Stay Safe and Stay Healthy !

End of Lecture 16